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EXAMINER	
KANG, DONGHEE	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 01/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/543,034	JIANG, TONGBI	
	Examiner	Art Unit	
	Donghee Kang	2811	

-- The MAILING DATE of this communication appears on the cover sh et with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2 and 3* is/are allowed.

6)☒ Claim(s) *1 and 4-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Allowable Subject Matter

1. The indicated allowability of claim 10 is withdrawn.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 10 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The phrase "**all of said electrical connection area is directly connected to at least one output electrical connection of said semiconductor device**" is not supported by disclosure. The disclosure describes only electrical connections (136) are attached between the electrical connection area (134) and traces (138), which are in electrical communication with electrical component either internal or external to the semiconductor substrate (104). See page 14, in lines 4-10. Thus, the electrical connection area (134) of this application is not directly connected the output electrical connection rather than through traces.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims **1, 4-5, 7, 9 & 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yew et al. (US 6,049,129) in view of APA (17).

Regarding claim **1**, Yew et al. disclose a semiconductor die assembly comprising (Figs. 4&5 and Col.8, lines 45 – Col.9, line7):

a printed circuit board (70; Col.8, lines 51-52) having a first surface (94) and a second surface (92), wherein said printed circuit board includes at least one opening (86; Col.8, line 62) defined therethrough between said printed circuit board first surface (94) and said printed circuit board second surface (92), wherein the printed circuit board is constructed from a material such as FR-4 (Col.3, lines 58-60 & Col.8, lines 53-54);

at least one semiconductor chip (50) having an active surface with at least one electrical connection area (120; Col.8, lines 59-60) disposed on said semiconductor chip active surface, said at least one semiconductor chip oriented having said at least one electrical connection area (120) substantially aligned with said at least one printed circuit board opening (86); and

at least one adhesive tape (60; Col.8, lines 47-50) interposed between and attaching said semiconductor chip active surface and said printed circuit board first surface (94), wherein a width of said at least one adhesive tape extends at least proximate an edge of said at least one semiconductor chip to an edge of said at least one printed circuit board opening.

The use of the phrase "semiconductor chip" and "semiconductor die" are considered to be interchangeable in the art. Thus, the "semiconductor chip" would meet the claimed phrase "semiconductor die".

The phrase "printed circuit board" would meet the claimed phrase "semiconductor substrate" because applicant noted that "the semiconductor substrate" can be an FR-4 printed circuit board (see disclosure; lines11-12 on page 13).

Yew et al. do not explicitly teach the electrical connection area disposed on said semiconductor die active surface directly connected to at least one output electrical connection of said semiconductor device. APA teaches in Fig.17 the electrical connection area (240) disposed on said semiconductor die active surface directly connected to at least one output electrical connection of said semiconductor device. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of APA into Yew's device in order to reduce manufacturing steps hence reducing cost.

Regarding claim **4**, Yew et al. disclose the semiconductor chip assembly further including at least one electrical connection (80) extending between said at least one electrical connection area (120) and at least strips (82) on said printed circuit board second surface (Col.8, lines 60-62). The phrase "strips" would meet the claimed phrase "trace" because the phrases, strips and trace, are often used interchangeable in the art.

Regarding claim **5**, Yew et al. disclose the at least one electrical connection comprises a bond wire (Col.8, lines 60-62).

Regarding claim **7**, Yew et al. disclose the semiconductor chip assembly further including a potting material (90) disposed within said at least one printed circuit board opening encasing said at least one electrical connection, wherein the potting material comprises epoxies or silicone (Col.7, lines 26-34 & Col.8, lines 65-66). The "potting material" would meet the claimed phrase "glob top material" because the phrase, potting material and glob top material, are often used interchangeable in the art, and the potting material and glob top material both include epoxy or silicone (see disclosure; lines18-20 on page 2).

Regarding claim **9**, Yew et al. disclose the at least one adhesive tape (60) comprises a planar carrier film (polyimide) including a first surface having a first adhesive disposed thereon and a second surface having a second adhesive disposed thereon (Col.3, lines 53-54).

Re claim **15**, Yew et al disclose a semiconductor die assembly, comprising (Figs. 4&5 & Col.8, lines 45 – Col.9, line7):

a printed circuit board (70; Col.8, lines 51-52) having a first surface (94) and a second surface (92), wherein said printed circuit board includes at least one opening (86; Col.8, line 62) defined therethrough between said printed circuit board first surface (94) and said printed circuit board second surface (92);

at least one semiconductor chip (50) having an active surface with at least one electrical connection area (120; Col.Col.8, lines 59-60) disposed on said semiconductor chip active surface, said at least one semiconductor chip oriented having said at least

one electrical connection area (120) substantially aligned with said at least one printed circuit board opening (86); and

at least one adhesive tape (60; Col.8, lines 47-50) interposed between and attaching said semiconductor chip active surface and said printed circuit board first surface (94), wherein a width of said at least one adhesive tape extends at least proximate an edge of said at least one semiconductor chip to an edge of said at least one printed circuit board opening.

The use of the phrase "semiconductor chip" and "semiconductor die" are considered to be interchangeable in the art. Thus, the "semiconductor chip" would meet the claimed phrase "semiconductor die".

The phrase "printed circuit board" would meet the claimed phrase "semiconductor substrate" because applicant noted that "the semiconductor substrate" can be an FR-4 printed circuit board (see disclosure; lines11-12 on page 13).

Yew et al. do not expressly teach that the semiconductor chip assembly is incorporated into a computer system. However, Yew et al. teach that the semiconductor chip (50) can be an integrated circuit component such as a DRAM, an EPROM or a SRAM (Col.3, lines 49-51). It is well known in the art that the computer system includes the memory chips, such as DRAM, EPROM, or SRAM. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the memory chips, such as DRAM, EPROM, or SRAM of Yew et al. into the computer system since the computer system is required to have a storage area to save information.

Yew et al. do not explicitly teach the electrical connection area disposed on said semiconductor die active surface directly connected to at least one output electrical connection of said semiconductor device. APA teaches in Fig.17 the electrical connection area (240) disposed on said semiconductor die active surface directly connected to at least one output electrical connection of said semiconductor device. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of APA into Yew's device in order to reduce manufacturing steps hence reducing cost.

6. Claim **6** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yew et al. in view of APA (Fig.15 & 17) and Khandros et al. (US 5,148,266).

Yew et al. do not expressly teach the electrical connection comprising a Tape Automate Bonding (TAB) connection. Khandros et al. note that the most widely utilized primary interconnection methods are wire bonding, tape automated bonding (TAB) and flip-chip bonding (Col.2, lines 23-25). Tape automated bonding (TAB) can provide the assembly with good resistance to thermal stresses (Col.3, lines 6-8). APA in Fig.15 also teaches a TAB connector (216) attached to bond pad (208) on the semiconductor chip and trace (212) on the semiconductor substrate. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the bond wire of Yew et al. with tape automated bonding (TAB) as taught by APA and Khandros since the tape automated bonding (TAB) can provide the semiconductor chip assembly with good resistance to thermal stresses.

7. Claim **8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yew et al. in view of APA (Fig.17) and further in view of Murakami et al. (US 5,612,569).

Yew et al. teach the semiconductor chip assembly further including an encapsulant material (90) encasing the back of semiconductor chip (50) (Col.7, lines 21-34 & Col.9, lines 2-3) but do not teach the encapsulant material encasing said glob top (potting) material and the principal surface of the semiconductor chip. However, Murakami et al. in Fig.34 teach the semiconductor chip having its principal surface covered with a glob top material (20) which is more flexible or fluid than the mold resin (2A) to cover the bonding wires while the outside being sealed up with a resin. Note that the circuit in the integrated package must be sealed to isolate it from the atmosphere, dirt, moisture, and other contamination which could destroy the circuit or affect its operation. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to mold the outside of the glob top (potting) material with a resin (encapsulant material) as taught by Murakami et al. in the Yew et al.'s device in order to protect the semiconductor package from contaminations.

8. Claims **11-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yew et al. in view of APA (Fig.17) and further in view of Boyko et al. (US 5,784,782).

Regarding claims **12 & 13**, Yew et al. teach substantially the entire claimed structure, as applied to claim 1 explained above, except that the semiconductor chip assembly further comprising at least one fillet located proximate said at least one

adhesive tape, said edge of said at least one semiconductor substrate opening, and said active surface of said at least one semiconductor die.

Applicant noted that filleting of the adhesive layers is caused by flow of the material in the adhesive layers during attachment of the semiconductor die to the semiconductor substrate by processing known in the art, such as heating processes, which cause the adhesive layers to momentarily flow out from the space between the carrier film and the semiconductor substrate and thereafter solidify (see disclosure; lines 18-23 on page 16).

Yew et al. also teach that the attachment of the semiconductor die (50) to the semiconductor substrate (70) is conducted under pressing and heating process (Col.4, lines 32-25). This pressing and heating process would cause the adhesive film to flow to and slightly within the base perimeter of the opening (86) and would form fillets located proximate the adhesive film, the printed circuit opening, and active surface of the semiconductor chip because the adhesiveness of the tape would stick to the surface of semiconductor die.

Even if this is not true, Boyko et al. (Fig.5 & Col.4, lines 32-42) teach that the heat and pressure cause the sticker sheet to bind ground plate to metallized dielectric layer (22) and cause the sticker sheet material to flow to and slightly within the base perimeter of the cavity (31). This leaves a fillet (82) of the sticker sheet material along the bottom perimeter of the cavity. This fillet has a smooth concave surface which minimizes stress concentrations and the tendancy to trap fluids or contaminants during subsequent processing.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form incorporate fillets of Boyko et al. into the Yew et al.'s device located proximate the adhesive film, the printed circuit opening, and active surface of the semiconductor chip since it minimizes stress concentrations and the tendancy to trap fluids or contaminants during subsequent processing.

Regarding claims **11 & 14**, Yew et al. teach substantially the entire claimed structure, as applied to claim 1 explained above, except that the semiconductor chip assembly further comprising at least one fillet located proximate said at least one adhesive tape, said edge of said at least one semiconductor chip, and said semiconductor substrate first surface.

Applicant noted that filleting of the adhesive layers is caused by flow of the material in the adhesive layers during attachment of the semiconductor die to the semiconductor substrate by processing known in the art, such as heating processes, which cause the adhesive layers to momentarily flow out from the space between the carrier film and the semiconductor substrate and thereafter solidify (see disclosure; lines 18-23 on page 16).

Yew et al. also teach that the attachment of the semiconductor die (50) to the semiconductor substrate (70) is conducted under pressing and heating process (Col.4, lines 32-25). This pressing and heating process would cause the adhesive film to flow to said edge of said at least one semiconductor chip and would form fillets located proximate the adhesive film, said edge of said at least one semiconductor chip, and said

semiconductor substrate first surface because the adhesiveness of the tape would stick to the surface of semiconductor die.

Even if this is not true, Boyko et al. teach that the heat and pressure cause the sticker sheet to bind ground plate to metallized dielectric layer 22 and cause the sticker sheet material to flow to and slightly within the base perimeter of the cavity 31. This leaves a fillet 82 of the sticker sheet material along the bottom perimeter of the cavity. This fillet has a smooth concave surface which minimizes stress concentrations and the tendancy to trap fluids or contaminants during subsequent processing. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form fillets located proximate said at least one adhesive tape, said edge of said at least one semiconductor chip, and said semiconductor substrate first surface in the Yew et al.'s device since it minimizes stress concentrations and the tendancy to trap fluids or contaminants during subsequent processing.

Allowable Subject Matter

9. Claims 2-3 are allowed.

Claim 10 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, first paragraph, set forth in this Office action.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 703-305-9147. The examiner can normally be reached on Maxiflex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on 703-308-1690. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Donghee Kang
Examiner
Art Unit 2811

dhk